

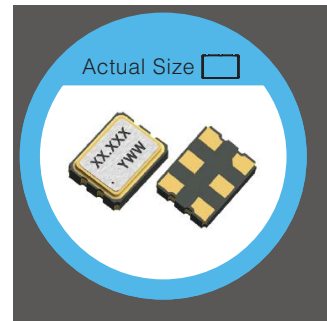
LE Type 3.2 x 2.5 mm SMD LVPECL/LVDS/ HCSL Crystal Oscillator

FEATURE

- Industry Standard 3.2 x 2.5 x 0.9 hermetically sealed ceramic package.
- Very low jitter performance: typical 0.1 pS RMS from 12 kHz - 20 MHz.
- Fundamental/3rd overtone crystal design.
- Output frequency up to 250 MHz.
- Tri-state enable/disable
- Up to 125°C operating temperature range.

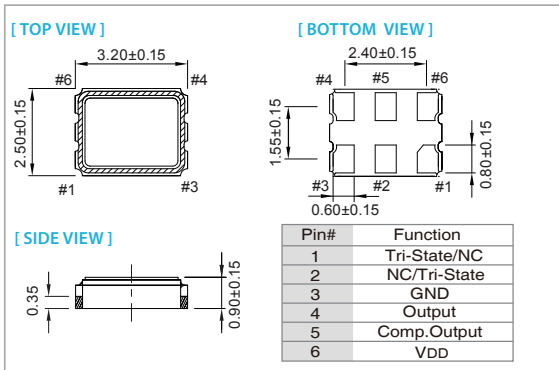
TYPICAL APPLICATION

- 10Gbit Ethernet, Fiber Channel, Storage Area Network, SONET
- Enterprise Servers, Reference clocks for ADC and DAC
- Telecom

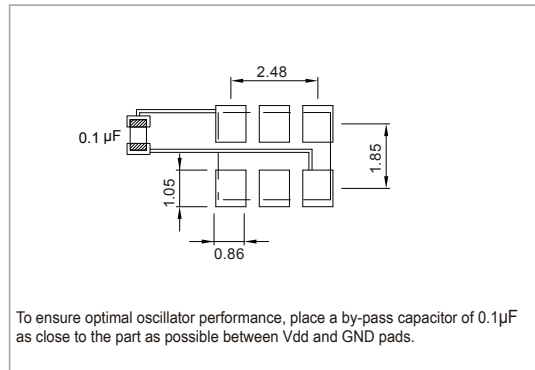


RoHS Compliant

DIMENSION (mm)



SOLDER PAD LAYOUT (mm)



ELECTRICAL SPECIFICATION

Parameter	LVPECL				LVDS				unit
	3.3 V		2.5 V		3.3 V		2.5 V		
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Supply Voltage Variation (V_{DD})	V _{DD} -5%	V _{DD} +5%	V _{DD} -5%	V _{DD} +5%	V _{DD} -5%	V _{DD} +5%	V _{DD} -5%	V _{DD} +5%	V
Frequency Range	10	250	10	250	10	250	10	250	MHz
Standard Frequency	25, 106.25, 125, 156.25, 161.1328, 212.5								
Supply Current	13.5 MHz ≤ F _o < 160 MHz		160 MHz ≤ F _o < 220 MHz		13.5 MHz ≤ F _o < 160 MHz		160 MHz ≤ F _o < 220 MHz		mA
Output Level	Output High		Output Low		Output High		Output Low		V
Transition Time: Rise/Fall Time*	-		1.0		-		1.0		nSec
Start Time	-		10		-		10		mSec
Tri-State(Input to Pin 2 or Pin 1)	Enable (High voltage or floating)		Disable (Low voltage or GND)		Enable (High voltage or floating)		Disable (Low voltage or GND)		V
RMS Phase Jitter (Integrated 12 KHz ~ 20 MHz)	F _o < 80 MHz		80 MHz ≤ F _o < 125 MHz		125 MHz ≤ F _o < 170 MHz		170 MHz ≤ F _o < 200 MHz		pSec
	200 MHz ≤ F _o		-		-		-		
	-		-		-		-		
	-		-		-		-		
Phase Noise@ 156.25 MHz	100 Hz		1 kHz		100 Hz		1 kHz		dBc/Hz
	-		-		-		-		
	-		-		-		-		
Aging (@ 25°C 1st year)	-		±3		-		±3		ppm
Storage Temp. Range	-55		125		-55		125		°C

Note: not all combination of options are available. Other specifications may be available upon request.

Specifications subject to change without notice.

Parameter	HCSL				unit
	3.3 V		2.5 V		
	Min.	Max.	Min.	Max.	
Supply Voltage Variation (VDD)	VDD-5%	VDD+5%	VDD-5%	VDD+5%	V
Frequency Range	25	175	25	175	MHz
Standard Frequency	100				
Supply Current 25 MHz ≤ Fo ≤ 175 MHz	–	50	–	50	mA
Output Level					V
Output High	0.6	–	0.58	–	
Output Low	–	0.15	–	0.15	
Transition Time: Rise/Fall Time+	–	0.5	–	0.5	nSec
Start Time	–	10	–	10	mSec
Tri-State(Input to Pin 2 or Pin 1)					V
Enable	0.7VDD	–	0.7VDD	–	
Disable	–	0.3VDD	–	0.3VDD	
RMS Phase Jitter (Integrated 12 kHz ~ 20 MHz)					pSec
25MHz ≤ Fo ≤ 175MHz	–	0.5	–	0.5	
Aging	–	±3	–	±3	ppm
Storage Temp. Range	-55	125	-55	125	°C

FREQ. STABILITY vs. TEMP. RANGE

Temp. (°C)	ppm	
	±25	±50
-10 ~ +60	○	○
-20 ~ +70	○	○
-40 ~ +85	△	○
-40 ~ +125	×	○

* ○ : Available △:Conditional X: Not available

* Inclusive of calibration @ 25 °C, operating temperature range, input voltage variation, load variation, aging (1st year), shock, and vibration

Note: not all combination of options are available. Other specifications may be available upon request.

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